In the Claims:

Claim 1 (Original): A method for use in reestablishing a timing signal in a high frequency timing circuit after the high frequency timing circuit has lost power, the method comprising:

(a) measuring the timing of a low frequency timing circuit against the timing of the high frequency timing circuit before the high frequency timing circuit has lost power,

(b) using the low frequency timing circuit to measure time after the high frequency timing circuit has lost power, and

(c) based on a time measurement obtained from the low frequency timing circuit, re-establishing the timing signal at an appropriate time after the high frequency timing circuit has regained power.

Claim 2 (Original): The method of claim 1, wherein measuring the timing of the low frequency timing circuit comprises measuring how many cycles of the high frequency timing circuit occur after a cycle of the timing signal begins and before a subsequent cycle of the low frequency timing circuit begins.

Claim 3 (Original): The method of claim 1, wherein using the low frequency timing circuit to measure time comprises measuring how many cycles of the low frequency timing circuit occur after the high frequency timing circuit has lost power.

Claim 4 (Original): The method of claim 1, wherein re-establishing the timing signal comprises:

(a) first allowing the high frequency timing circuit to generate the timing signal after the high frequency timing circuit has regained power, and

(b) repositioning the timing signal based upon the time measurement obtained from the low frequency timing circuit.

Claim 5 (Original): The method of claim 1, wherein reestablishing the timing signal comprises:

(a) first using the low frequency timing circuit to reapply power to a high frequency oscillator that drives the high frequency timing circuit, and then

(b) using the low frequency timing circuit and a signal from a high frequency oscillator to generate a synchronization pulse that aligns the high frequency timing signal.

Claim 6 (Original): An electronic device comprising:

(a) a high frequency timing circuit configured to produce a timing signal,

(b) power-down circuitry configured to remove power temporarily from the high frequency timing circuit,

(c) a low frequency timing circuit configured to measure time after the high frequency timing circuit has lost power,

(d) calibration circuitry configured to measure the timing of the low frequency timing circuit against the timing signal before the high frequency timing circuit has lost

power, and

(e) control circuitry configured to receive a time measurement from the low frequency, timing circuit and reestablish the timing signal at an appropriate time after the high frequency timing circuit has regained power.

Claim 7 (Original): The electronic device of claim 6, wherein the calibration circuitry includes counting circuitry configured to measure how many cycles of the high frequency timing circuit occur after a cycle of the timing signal begins and before a subsequent cycle of the low frequency timing circuit begins.

Claim 8 (Original): The electronic device of claim 6, wherein the calibration circuitry includes circuitry configured to count a high frequency oscillator beginning on a certain cycle of a low frequency oscillator, and to produce a synchronization pulse after a certain number of cycles of a high frequency oscillator have elapsed.

Claim 9 (Original): The electronic device of claim 6, wherein the low frequency timing circuit includes counting circuitry configured to maintain a continuous count of low frequency clock cycles after the high frequency timing circuit has lost power.

Claim 10 (Original): The electronic device of claim 6, wherein the control circuitry is configured to:

(a) allow the high frequency timing circuit to generate the timing signal after regaining

power, and then

(b) reposition the timing signal based upon the time measurement obtained from the low frequency timing circuit.

Claim 11 (Original): The electronic device of claim 6, wherein the control circuitry is configured to:

(a) first using the low frequency timing circuit to reapply power to a high frequency oscillator that drives the high frequency timing circuit, and then

(b) using the low frequency timing circuit and a signal from a high frequency oscillator to generate a synchronization pulse that aligns the high frequency timing signal.

Claim 12 (Original): The electronic device of claim 6, further comprising means for automatic recovery of time, day and date information from a base station.

Claim 13 (New): A method for use by a mobile station to synchronize a high frequency timing circuit to a frame pulse used for synchronizing the mobile station with a base station in a wireless network, the method comprising:

calibrating a timing of a low frequency timing circuit against a timing of the high frequency timing circuit;

entering the high frequency timing circuit into a sleep mode;

waking up the high frequency timing circuit from the sleep mode in response to a wake up signal generated by the low frequency timing circuit; and

synchronizing the high frequency timing circuit, after the waking up, to the frame pulse based on the timing of the low frequency timing circuit.

Claim 14 (New): The method of claim 13, wherein prior to the synchronizing and after the waking up, the method further comprises: generating a first frame pulse using the high frequency timing circuit.

Claim 15 (New): The method of claim 14, wherein the synchronizing includes calculating an arrival time of the first frame pulse, determining a time offset using the arrival time, and re-programming the high frequency timing circuit using the time offset.

Claim 16 (New): The method of claim 15, wherein the calculating of the arrival time uses the timing of the low frequency timing circuit.

Claim 17 (New): The method of claim 13, wherein prior to the entering of the high frequency timing circuit into the sleep mode, the method further comprises: calculating a time offset indicative of a time between when the wake up signal is to be generated by the low frequency timing circuit and when a next frame pulse is to be generated; and generating the frame pulse by the high frequency timing circuit using the time offset.